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[0019] An arbiter may be used with a processor in a point-to-point architecture to allow a customer to change the number of ports linked between a processor and a device external to the processor. A point-to-point bus architecture provides an uninterrupted connection between two separate devices. Generally, a packet based protocol transfers information in a point-to-point bus architecture. The arbiter may alter the number of ports linked between the processor and the device exterior to the processor by changing one or more internal signal pathways in the processor without changing a physical component layout in the processor. In an embodiment, the manufacturer or the customer may change the number of ports linked between the two devices to increase the bandwidth between the devices. In an embodiment, the manufacturer or the customer may add additional processors linked to a device by changing the number of ports linked between a first processor and the device exterior to the first processor.

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processor **200** has an arbiter **202** and three layers, the protocol layer **204**, a buffer layer **206** such as one or more link layers **210**, and an information transfer layer **208** such as one or more physical layers **212**. The arbiter **202** changes the signal pathways within the physical layer **212** and link layer **210** without changing the physical component layout in the processor **200**. The physical layer **212** carries out the actual physical transfer of information to and from other devices. The link layer **210** performs liaison functions between the higher functions of the protocol layer **204** and the physical layer **212**. The protocol layer **204** processes requests, responses, and data transfers.

[0021] In an embodiment, the arbiter **202** may be internal or external to the processor **200**. In an embodiment, a single arbiter **202** controls the signal pathways in all the layers of the processor **200**. In an alternative embodiment, multiple arbiters **202** exist to control the signal pathways. The arbiter **202** may be a combination of hardware and software. The arbiter **202** may have several functions such as sending an enable/disable signal to one or more signal pathway switching devices and sending a signal to change various clocking speeds. The buffer layer **206** may have one or more inbound signal pathways. The buffer layer **206** may have one or more outbound signal pathways. The information transfer layer **208** may have one or more inbound signal pathways. The information transfer layer **208** may have one or more outbound signal pathways.

[0022] Figure 3 illustrates a two processor point-to-point architecture **300** having a 16-bit point-to-point connection between: 1) an input-output component **302** and the first processor **304**; as well as 2) the input-output component **302** and the second processor **306**. A first



processor **304** having four 16-bit ports **308, 310, 312, 314** connected to the processor may have three 16-bit ports **308, 310, 312** connected to a second processor **306** and one 16-bit port connected **314** to the input-output component **302**. In an embodiment, the input-output component maybe a bridge, a memory, a chipset or similar component. Thus, a 48-bit bandwidth connection exists between the first processor **304** and the second processor **306**. Further, the first processor **304** and the second processor **306** have a 16-bit bandwidth connection to the input-output component **302**. The arbiter can change the signal pathways in the first processor **304** such that the processor now has two 16-bit point-to-point (32-bit) connections to the second processor **306** and a 32-bit connection to the input-output component **302**.

[0023] Figure 4 illustrates a two processor point-to-point architecture **400** having a 32-bit point-to-point connection between: 1) the input-output component **402** and the first processor **404**; as well as 2) the input-output component **402** and the second processor **406**. A first processor **404** having four 16-bit ports **408, 410, 412, 414** connected to the processor may have two 16-bit ports connected to a second processor **406** and two 16-bit ports connected to the input-output component **402** such as a chip set. Thus, a 32-bit bandwidth connection exists between the first processor **404** and the second processor **406**. Further, the first processor **404** and the second processor **406** have a 32-bit bandwidth connection to the input-output component **402**. In the 32-bit mode as compared to 16-bit mode, the bandwidth between the input-output component **402** and the first processor **404** as well as the input-output component **402** and the second processor **406** has effectively doubled. Bandwidth is the total amount of information that can be transferred within a given time period between two devices. In 16-bit mode, eight clock cycles

must occur to transfer eight 16-bit packets (128 bits) of information between each processor and the input-output component. In 32-bit mode, four clock cycles must occur to transfer four 32-bit packets (128 bits) of information between each processor and the input-output component.

[0024] Figure 5 illustrates an embodiment of a four processor point-to-point architecture **500** having a 16-bit point-to-point connection between an input-output component **502** and each of the four processors **504, 506, 508, 510**. The four processors are processor 1 **504**, processor 2 **506**, processor 3 **508**, and processor 4 **510**. In an embodiment, each of the four processors **504, 506, 508, 510** employs an embodiment of the arbiter. The processors **504, 506, 508, 510** have a flexible architecture that coordinates with the arbiter to allow a variety of uses for these processors **504, 506, 508, 510**. For example, the four processor architecture **500** may be substituted with the two processor architecture employing a 32-bit connection with the input-output component **502**. Thus, the processing power of this arrangement has effectively doubled because four processors will process the data coming from the input-output component **502**. Thus, an embodiment of the arbiter allows the same input-output component **502** to work with either a two processor architecture, a four processor architecture **500** or other similar multiple processor architecture.

[0025] A programmable knob setting in a configuration register directs the arbiter to establish the customer's current desired configuration such as a 16-bit, 32-bit, or 48-bit point-to-point connection between the processor and a device exterior to the processor. In an embodiment, the device exterior to the processor may be another processor, an input-output device, a bridge or other similar device. In an embodiment, the manufacturer or the customer may program the knob



processor **610** through eighth processor **612** eventually link with the chipset **630**. In an embodiment, the arbiter may allow the signal paths internal to each processor **602, 604, 606, 608, 610, 612, 614** and **616**, to be changed by a programmable setting. This allows a manufacturer to fabricate a single version of a processor with a generic but flexible architecture within the processor to service multiple processor platforms. Thus, in an embodiment, an arbiter linked to a processor having a single flexible architecture may be employed to service, a 2P architecture, 4P architecture, 8P architecture or other multiple processor architecture, as well as service a server application and a workstation application.

[0028] In an embodiment, the ability of the arbiter to change the allocation of internal signal paths allows a manufacturer to design and fabricate fewer versions of the same chip to service customers needs. In an embodiment, the architecture of the processor is the arrangement and component makeup of the various elements within the processor. In an embodiment, the components and elements contained within the protocol layer, the information layer and the buffer layer makeup the architecture of the processor. Those ordinarily skilled in the art will recognize the specific components illustrated in the following embodiments may be deviated from and still be within the spirit of this invention.

[0029] Figure 7 illustrates an embodiment of the arbiter **702** controlling the inbound signal pathways in an embodiment of the information transfer layer **700**. The first physical layer (SPXO) **704** has a first port **706**; nine 16-bit registers, a first register **708**, a second register **710**, a third register **712**, a fourth register **714**, a fifth register **716**, a sixth register **718**, a seventh register **720**, an eighth register **722**, and a ninth register **724**; first 64-bit register **726**; a signal pathway



[0031] If the configuration register 754 is programmed for a 32-bit point-to-point connection, then the arbiter 702 gangs two physical layers to act together. The arbiter 702 disables the 128-bit path in the first signal pathway switching device 728. The arbiter 702 enables the dual 64-bit path in the first signal pathway switching device 728. The arbiter 702 enables the first flip flop 730 but disables the second flip flop 756. The arbiter 702 increases the clocking speed for the first register 708 through the eighteenth register 752 by a factor of two. The first physical layer 704 receives four 16-bit packets of information and stores the packets of information in the second register 710 through the fifth register 716. The second physical layer 732 receives four 16-bit packets of information and stores the packets of information in the eleventh register 738 through the fourteenth register 744. The first signal pathway switching device 728 senses that the first 64-bit register contains four 16-bit packets of information from the second register 710 through the fifth register 716. The first signal pathway switching device 728 senses that the second 64-bit register contains four 16-bit packets of information from the eleventh register 738



[0033] In an embodiment of the inbound buffer layer **800**, if the configuration register **832** is programmed for a 32-bit point-to-point connection, then the arbiter **802** effectively gangs two link layers together. The first link layer **804** receives the eight related 16-bit packets (128-bit) of information at twice the clock speed from the communication switching device in the first physical layer. The first link layer **804** stores the 128-bit packet of information in the first register **806**. The 128-bit packet of information is routed appropriately to either the first response queue **808** or the first request queue **810**. The arbiter **802** sends an enablement signal to the first signal pathway switching device **812**, third signal pathway switching device **834**, and fifth signal pathway switching device **822**. The arbiter **802** also sends a disable signal to the second signal pathway switching device **816** and fourth signal pathway switching device **836**. The arbiter **802** directs the fifth signal pathway switching device **822** to request data only from the first signal pathway switching device **812** and the third signal pathway switching device **834**. In 32-bit mode, the second signal pathway switching device **816** and fourth signal pathway switching device **836** receive no signal from the physical layer because the arbiter **802** disabled the second flip flop and fourth flip flop in the physical layer.

[0034] The 128-bit packets of information are transferred to the fifth signal pathway switching device **822** through the first signal pathway switching device **812** and then the third signal pathway switching device **834** in a cyclic sequential manner. In a repeating cycle, the fifth signal pathway switching device **822** requests the contents of the first response queue **808**, then the first request queue **810**, then the third response queue **838**, then the third request queue **840**, and then repeats this sequence. Every packet of information may be either a request for a command and/or data or a response to a command or data. In an embodiment, once a packet is written into a



[0035] If the configuration register **832** is programmed for a 16-bit point-to-point connection, then each inbound link layer **804, 814, 818, 820** acts independently. The arbiter **802** directs the fifth signal pathway switching device **822** to request information out of the eight possible sources, the corresponding request queue **810, 813, 840, 850** or the corresponding response queue **808, 811, 838, 848** in each link layer **804, 814, 818, 820**, in a cyclic sequential manner. If a particular queue is empty, then the fifth signal pathway switching device **822** automatically pulls packets out of the next queue without any penalty. In an embodiment, the packets from the four physical layers are written into the appropriate queue at 100 megahertz, if the configuration register is programmed for a 16-bit connection. The packets are written into the queues at 200 Megahertz if the configuration register **832** is programmed for a 32-bit connection. If the configuration register is configured for a 48-bit connection, then the arbiter **802** gangs three link layers together. Once the fifth signal pathway switching device **822** picks a packet of information from one of the eight possible sources, then the packet is sent to the to the protocol

layer **840**.

[0036] The inbound link layer sends responses and requests to protocol layer **840**. The protocol layer **840** alternates choosing a command from the LATT **826** or RATT **830** accompanied by data from the CDM **828**. In one embodiment, this physical information may be sent to a CPU. The information goes to the CPU to be processed and sent to the outbound bound link layer. The protocol layer **840** typically is the processing component. The protocol layer **840** typically resolves requests from other local processors and sends requests out through the physical layer. The protocol layer **840** may be responsible for functions such as ordering, conflict detection, and coherence. The protocol layer **840** may forward requests for data to the local memory controller if the request is made to local memory. The protocol layer **840** may send snoop requests to the remote nodes and other local processors. The protocol layer **840** also processes requests made through the link layer, which may come from a remote processor or an input-output component.

[0037] Figure 9 illustrates an embodiment of the arbiter **902** controlling the outbound signal pathways in an embodiment of the buffer layer **900**. The protocol layer **904** sends the processed data and commands to each outbound link layer **906**, **908**, **910**, **912**. The protocol layer **904** delivers commands generated from itself to the LATT **914** and data, if any, corresponding to that command to the CDM **916**. The protocol layer **904** delivers responses to commands from remote devices to the RATT **918** and data, if any, corresponding to that command to the CDM **916**. If the configuration register **920** is programmed for a 32-bit point-to-point connection, then the arbiter **902** effectively enables two of the four outbound link layers. The following happens in

tracing the signal path in the first outbound link layer **906** and the second outbound link layer **908**. The arbiter **902** directs the second signal pathway switching device **922** and the fourth signal pathway switching device (not shown) to be disabled. The arbiter **902** directs the fifth signal pathway switching device **928** to request data through the first signal pathway switching device **924** and third signal pathway switching device **926** from their respective request buffer **930** or response buffer **932**. The fifth signal pathway switching device **928** alternates, in a repeating cycle, requests for bits from the request buffer **930** and the response buffer **932**. The fifth signal pathway switching device **928** also receives any data, if any, corresponding to those commands from the CDM **916**. The fifth signal pathway switching device **928** then routes the 128-bit data packet through a first time delay **933** to either the outbound response queue **936** or outbound request queue **934** located in the outbound physical layer.

[0038] One or more retry queues **938** exist in the outbound link layer. The retry queue **938** stores a duplication of the information to be transferred in case an error occurs in the transfer of the information. The retry queue **938** exists primarily in case there may be an error in the link. The retry queue **938** erases the duplicated information stored in a retry queue **938** upon receiving a confirmation of an error free transfer of information.

[0039] If the configuration register **920** is programmed for a 16-bit point-to-point connection, then the arbiter **902** directs each outbound link layer **906**, **908**, **910**, **912** to act independently. The arbiter **902** sends a signal to enable all of the outbound link layer communication switching devices and set the clock speed to the default clock speed. The information is routed from the LATT **914**, RATT **918**, and CDM **916** through its own respective outbound link layer to the corresponding outbound physical layer. For example, the arbiter **902** directs the second signal



the 128-bit packet of information from either the response queue **1011** or the request queue **1010** at a clock speed of 100 megahertz for example. The signal output of the first signal pathway switching device **1008** is two 64-bit packets of information, a first 64-bit packet and a second 64-bit packet which are stored in the first register **1012**. After a time delay **1014**, the second signal pathway switching device **1018** reads the first 64-bit packet through the second register **1016** at twice the clock speed, 200 megahertz, of the 128-bit packet of information. The signal output of the second signal pathway switching device **1018** is two 32-bit packets of information, a first 32-bit packet and a second 32-bit packet which are stored in the third register **1020**. The clock speed of 32-bit packet of information in the third register is again doubled to 400 megahertz.

[0042] The arbiter **1002** now directs the 32-bit packet of information to take a 32-bit bypass path **1022** or a 16-bit information transfer path in the corresponding signal pathway switching devices **1026**, **1034**. The configuration register **1024** informs the arbiter **1002** whether the component exterior to the processor should be a 16-bit, 32-bit or 48-bit-point-to-point connection. In one embodiment, for example, if a 16-bit point-to-point connection exists between the processor and the input-output component, then arbiter **1002** directs each physical layer to act independently of the other physical layers. A fourth signal pathway switching device **1026** reads the 32-bit packet of information at 400 megahertz from the third register **1020** and outputs two 16-bit packets of information. A fifth signal pathway switching device **1028** reads the 16-bit packet of information at 400 megahertz from the forth register **1027** and outputs the 16-bit packet of information to the first port **1004**. The arbiter **1002** sends a signal to the sixth signal pathway switching device **1030** in the second outbound physical layer **1032**. The signal enables the 16-bit path in the fifth signal pathway switching device **1028**. The arbiter **1002**

disables the 32-bit bypass path **1022** from the fourth signal pathway switching device **1026**. The arbiter **1002** also sends a signal to the second physical layer **1032**, the sixth signal pathway switching device **1030**, to enable the 16-bit path in the sixth signal pathway switching device **1030** and disable/ignore the 32-bit bypass path **1022** coming from the third register **1020**. Thus, the output from first port **1004** and the second port **1006** are unrelated 16-bit packets of information.

[0043] If in one embodiment for example, a 32-bit point-to-point connection exist between the processor and the input-output component, then the arbiter **1002** gangs the output of the first port **1004** and the output of the second port **1006**. The arbiter **1002** sends a signal to the sixth signal pathway switching device **1030**. The arbiter's signal disables the 16-bit path in the sixth signal pathway switching device **1030** and enables the 32-bit bypass path **1022** coming from the third register **1020**. The arbiter **1002** also sends a signal to the first physical layer **1031**, the fourth signal pathway switching device **1026**, to enable the 32-bit bypass path **1022**. Thus, the output from first port **1004** and the second port **1006** are related 16-bit packets of information. In other words, the output from first port **1004** and the second port **1006** is a 32-bit packet of information. In order to keep the same transfer speeds, the arbiter **1002** also sends a signal to double the clocking speed that occurs in the registers. For example, the 32-bit packet of information in the third register **1020** is now clocked at 800 megahertz. 800 megahertz is twice the clock speed of when the 16-bit information transfer was occurring. In a similar manner, the arbiter **1002** can gang three ports together (not shown) to create a 48-bit connection in the outbound path.

[0044] In alternative embodiment, if three physical layers are linked to, for example, a second processor, then optionally the arbiter can be programmed to route the three related 16-bit packets

